TER-010

002260"2687960

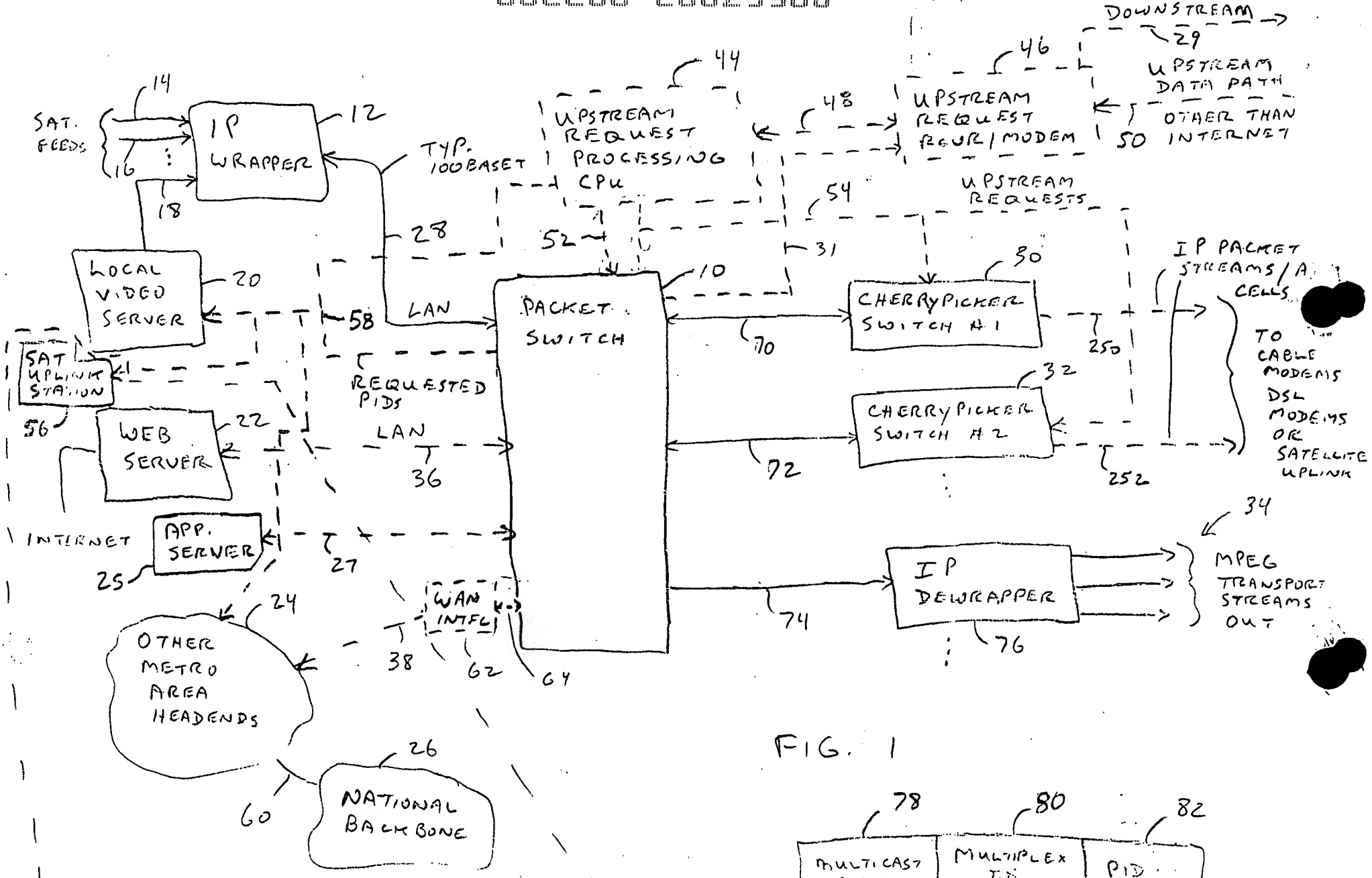
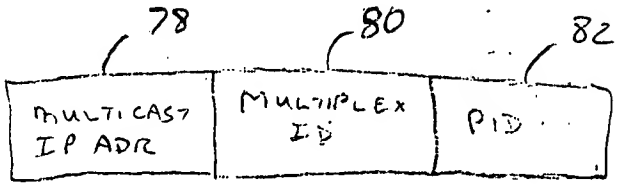


FIG. 1



IP WRAPPER GENERATED MULTICAST IP ADDRESS

FIG. 2

PROCESS OF ENCAPSULATION CARRIED OUT IN IP WRAPPER FPGA

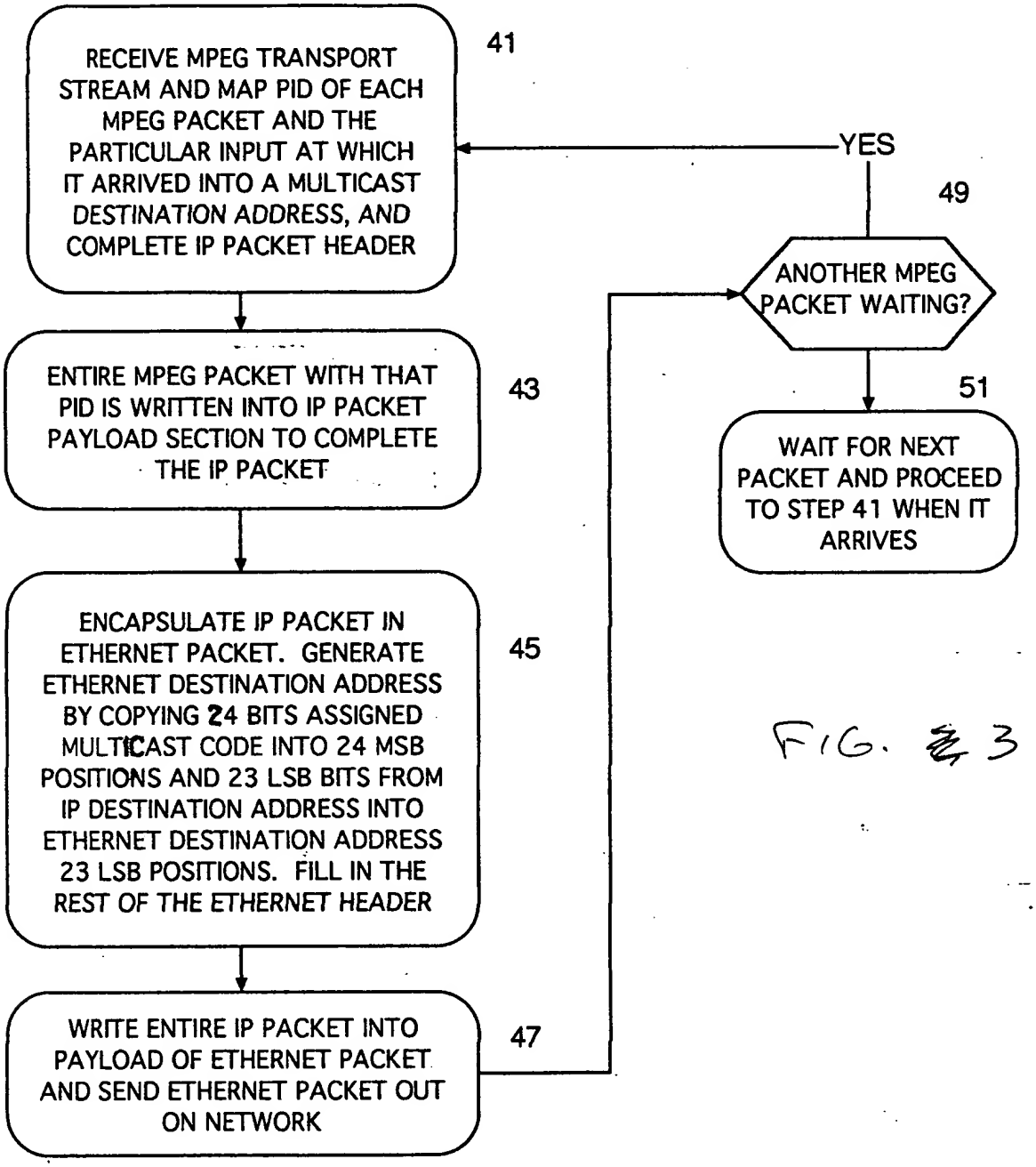


FIG. 3

09609892 - 062200

PREFERRED ENCAPSULATION PROCESS CARRIED OUT BY IP WRAPPER

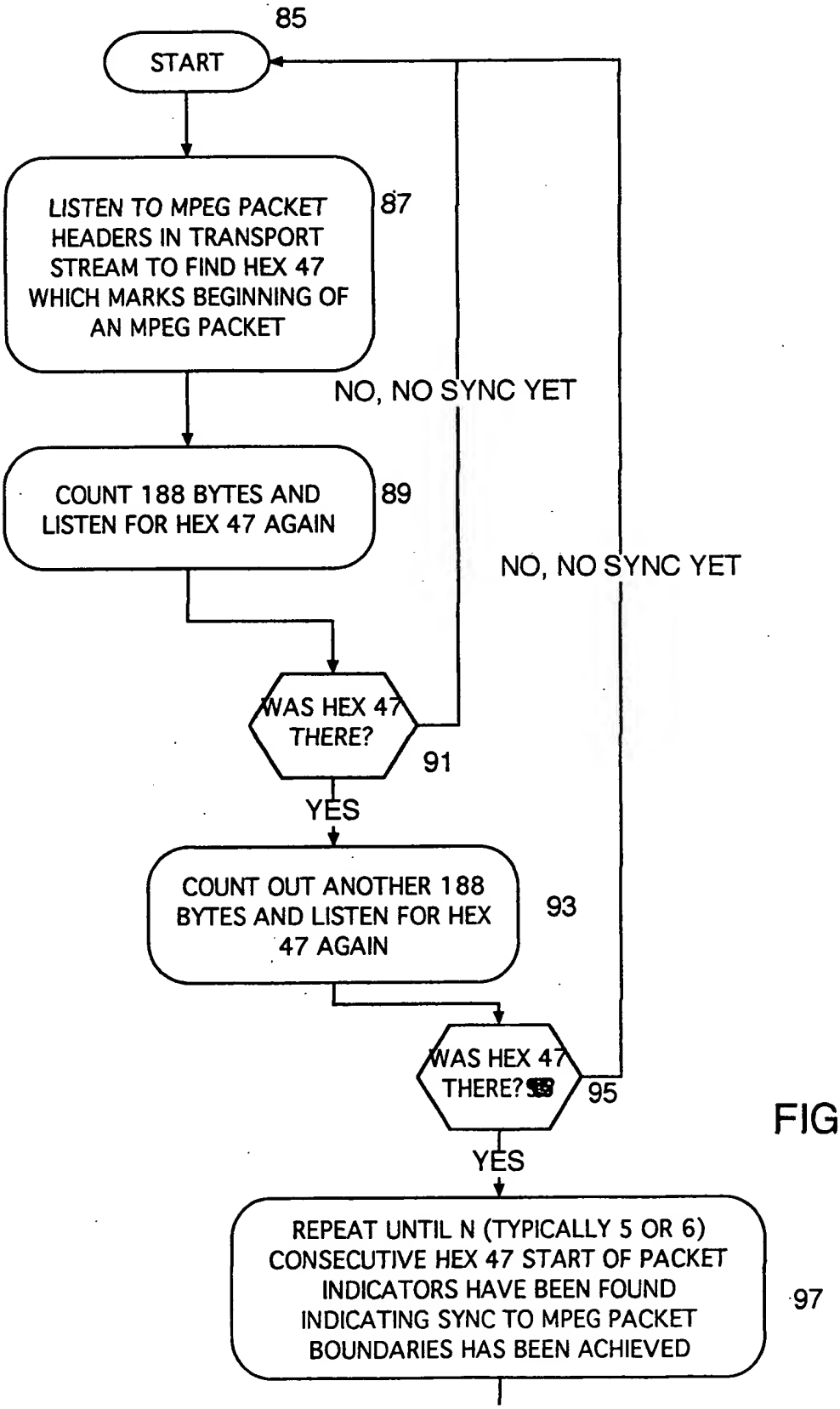


FIG. 4A

DOCSNY\88502.0020

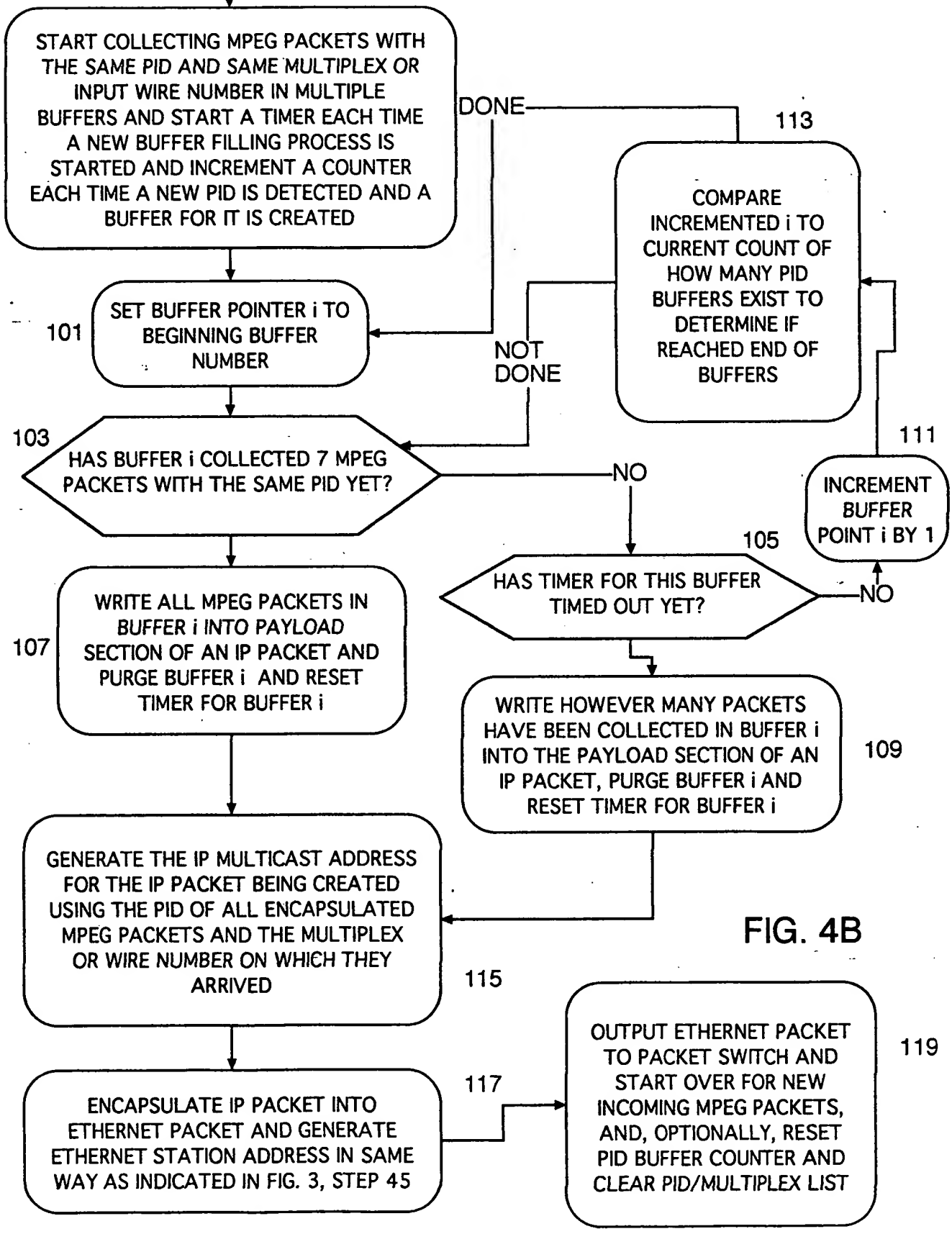


FIG. 4B

Docket: 50020000

PROCESS OF GENERATING MPEG TRANSPORT STREAMS IN CHERRYPICKER SWITCHES

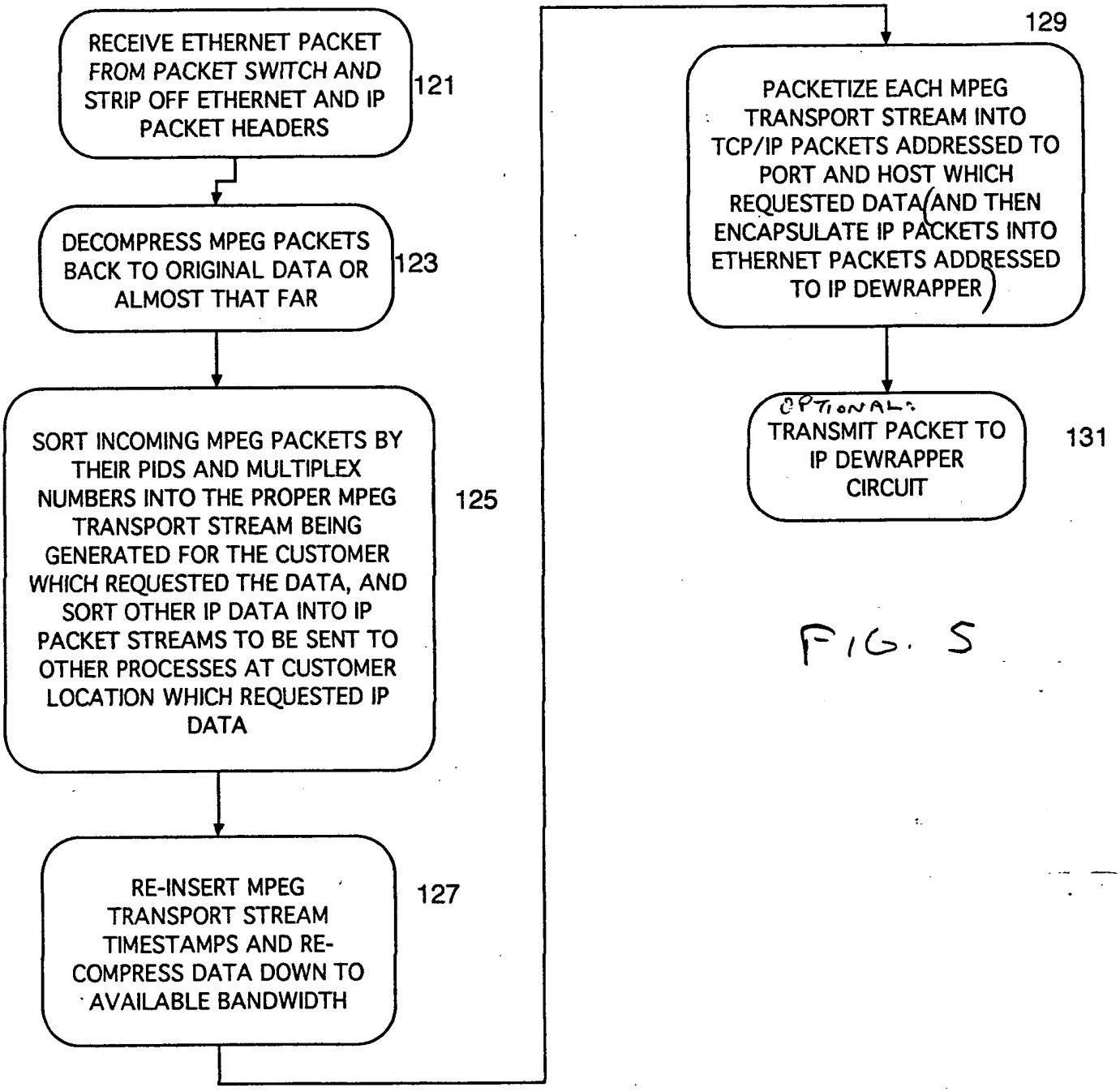
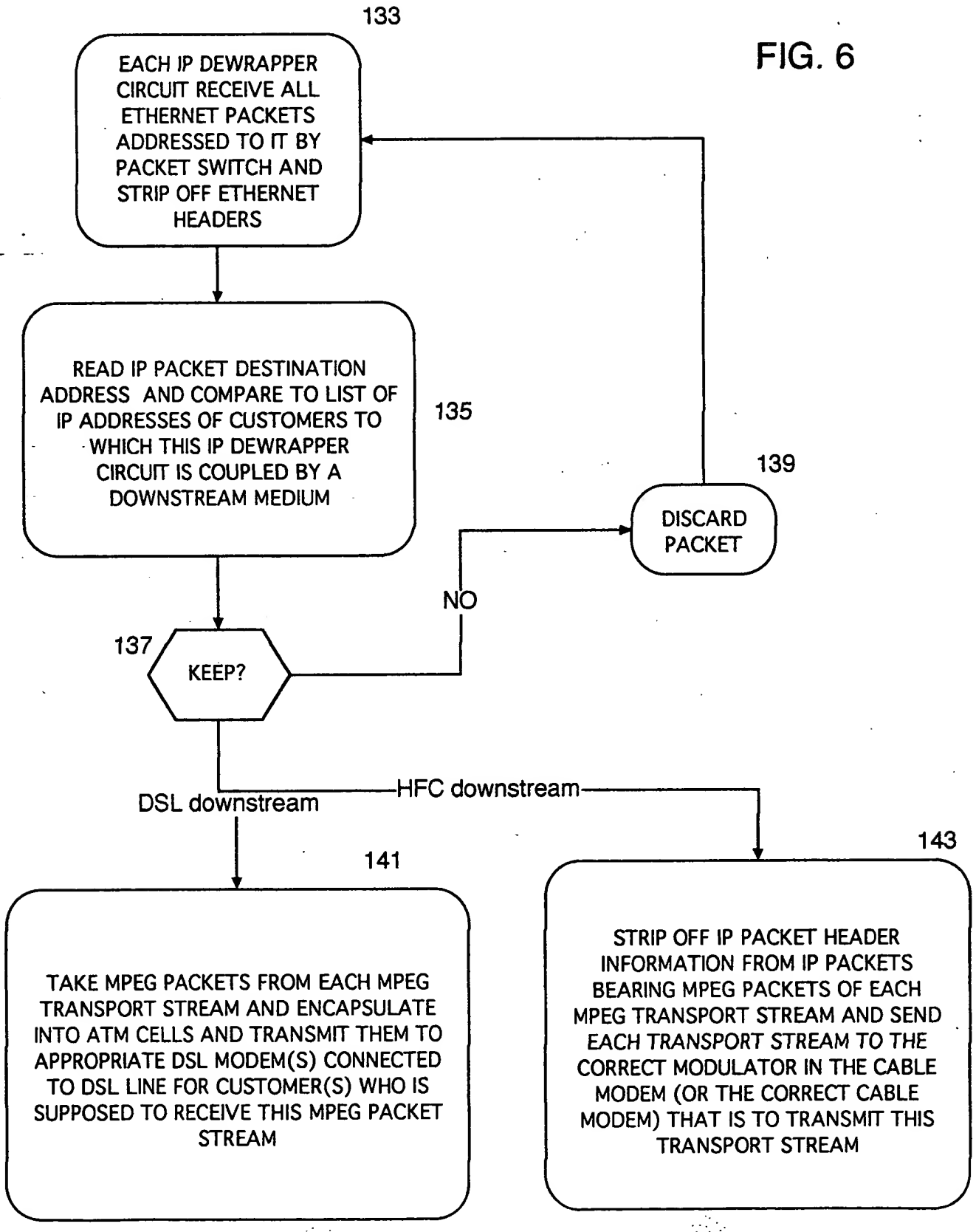


FIG. 5

0000000-0000000

IP DEWRAPPER PROCESS FOR DSL OR HFC ENVIRONMENTS

FIG. 6



09609302.060200

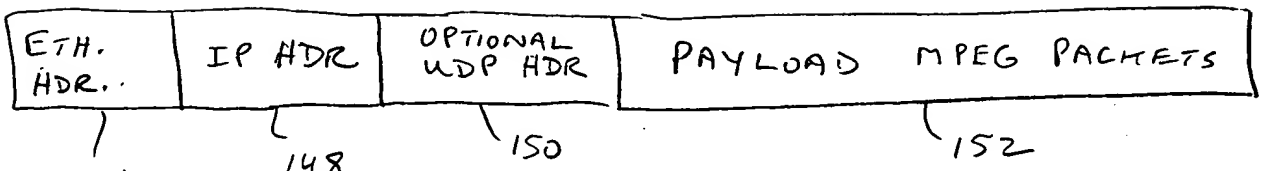

ETH. HDR.
IP HDR
OPTIONAL UDP HDR
PAYLOAD MPEG PACKETS
146
148
150
152

FIG. 7

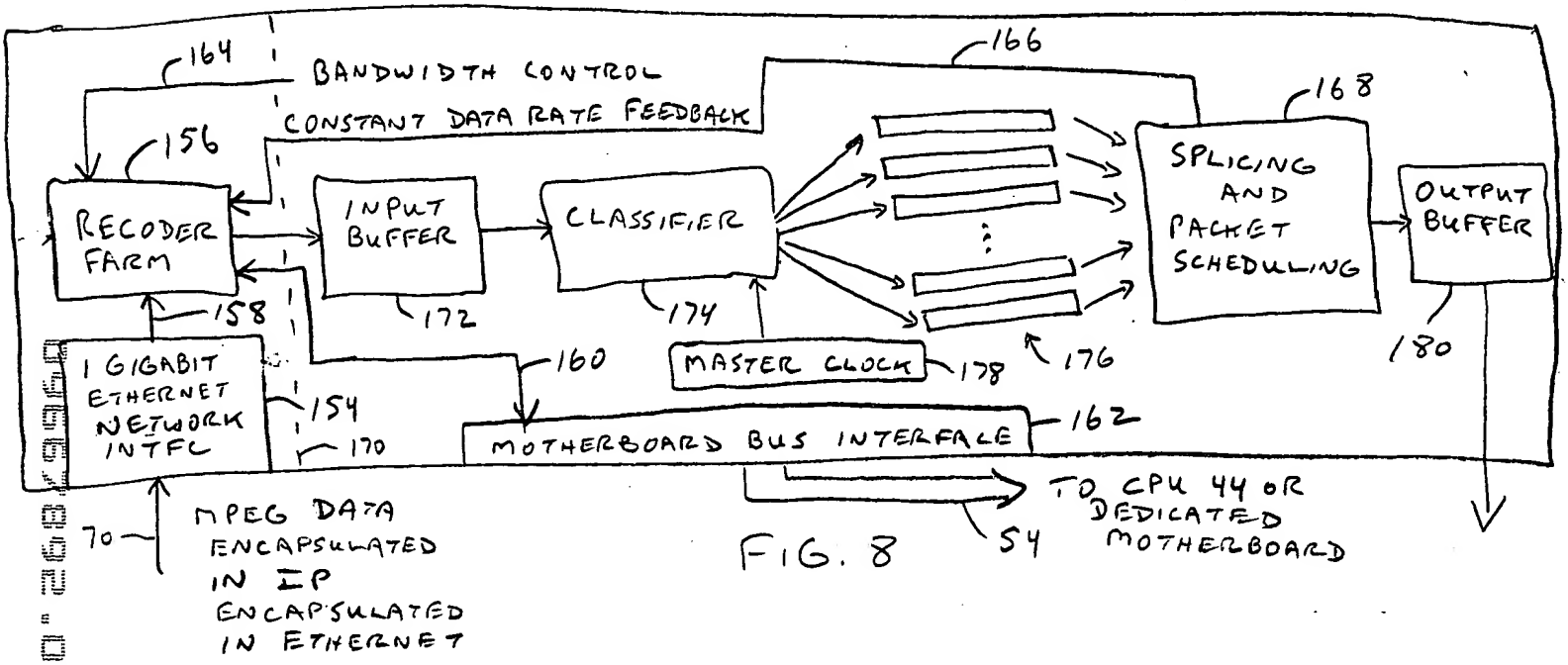

164
BANDWIDTH CONTROL
CONSTANT DATA RATE FEEDBACK
166
168
156
RECODER FARM
INPUT BUFFER
CLASSIFIER
SPLICING AND PACKET SCHEDULING
OUTPUT BUFFER
158
172
174
176
180
1 GIGABIT ETHERNET NETWORK INTFC
154
170
160
MASTER CLOCK
178
MOTHERBOARD BUS INTERFACE
162
70
MPEG DATA ENCAPSULATED IN IP ENCAPSULATED IN ETHERNET
TO CPU 44 OR DEDICATED MOTHERBOARD
54

FIG. 8

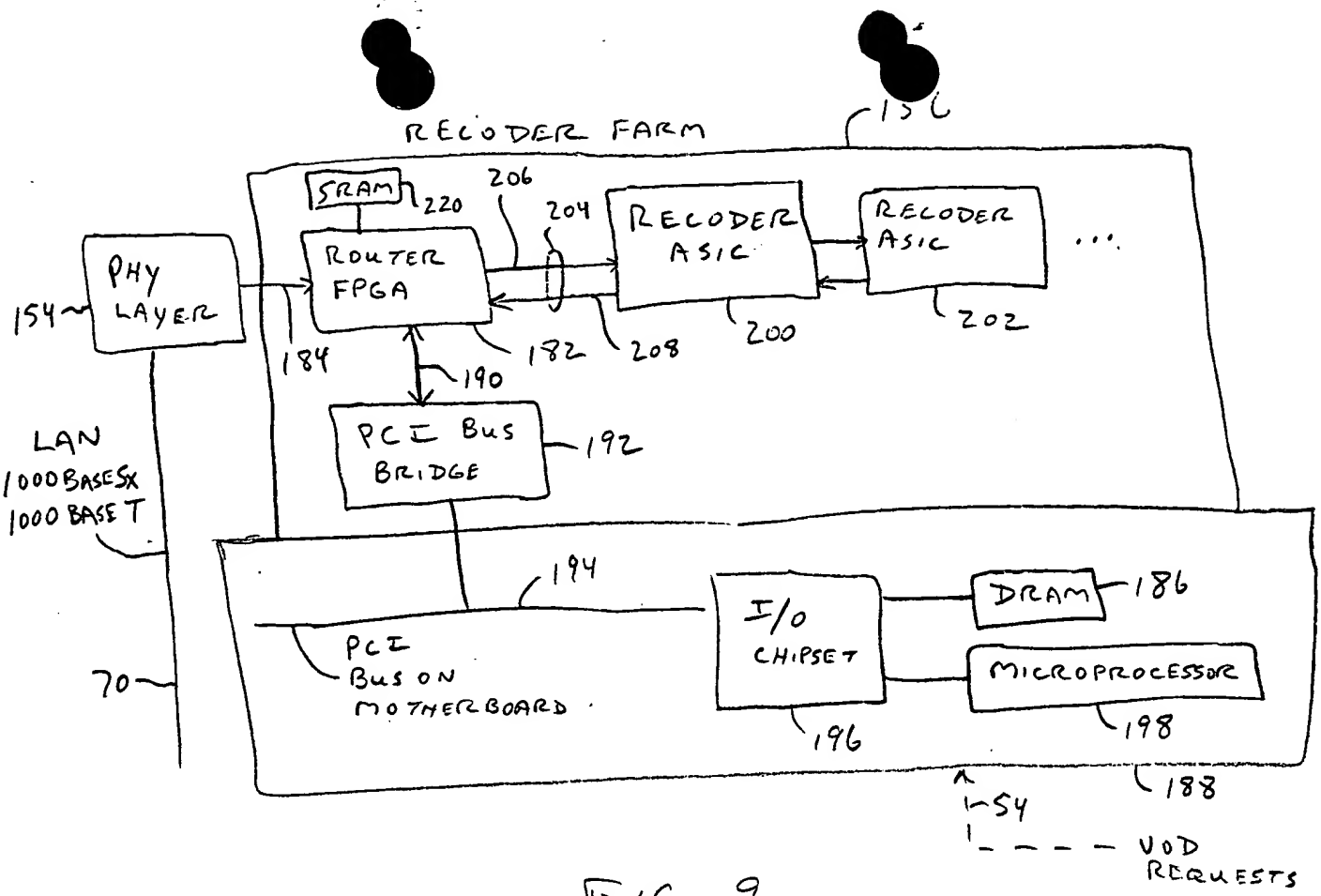

RECODER FARM
156
SRAM
220
206
204
RECODER ASIC
RECODER ASIC
ROUTER FPGA
PHY LAYER
154
184
182
208
200
202
190
PCI BUS BRIDGE
192
LAN
1000BASESX
1000 BASE T
194
I/O CHIPSET
DRAM
186
PCI BUS ON MOTHERBOARD
70
MICROPROCESSOR
196
198
188
54
VOD REQUESTS

FIG. 9

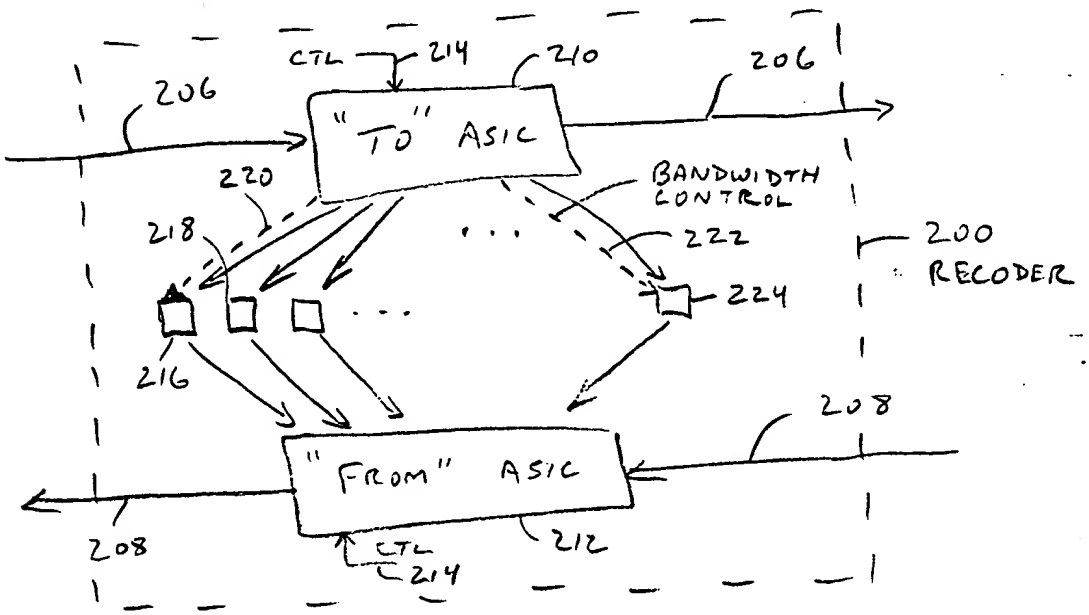

CTL
214
210
206
206
"TO" ASIC
220
BANDWIDTH CONTROL
218
222
200
RECODER
224
216
208
"FROM" ASIC
208
CTL
214
212

FIG. 10

HEADEND ARCHITECTURE TO SEND DATA AND VOD AND/OR BROADCAST DATA TO CUSTOMERS VIA HFC

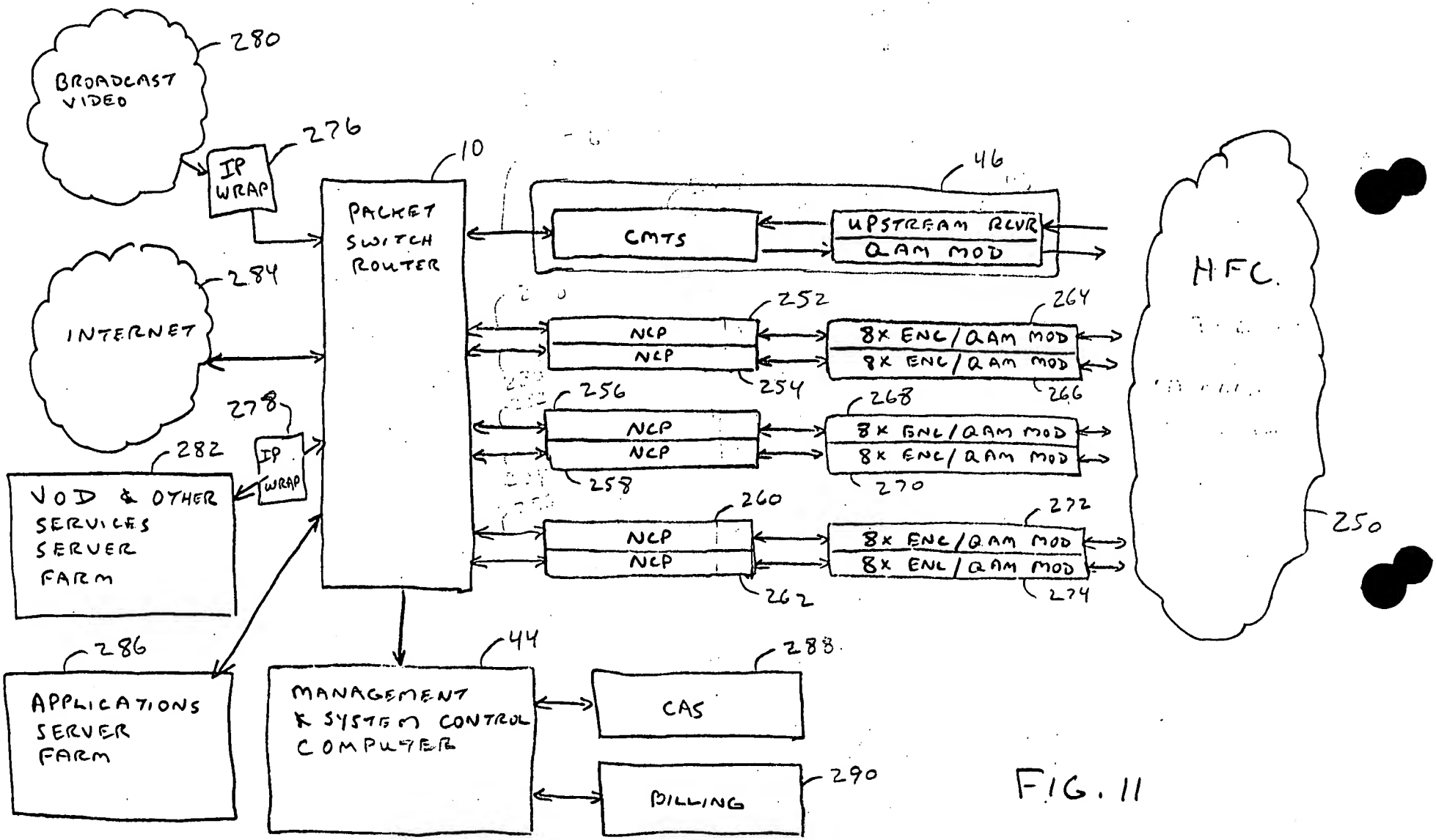


FIG. 11

EMBODIMENT FOR TRANSMISSION OF DATA AND VIDEO PROGRAM DATA FROM HEADEND TO CUSTOMERS

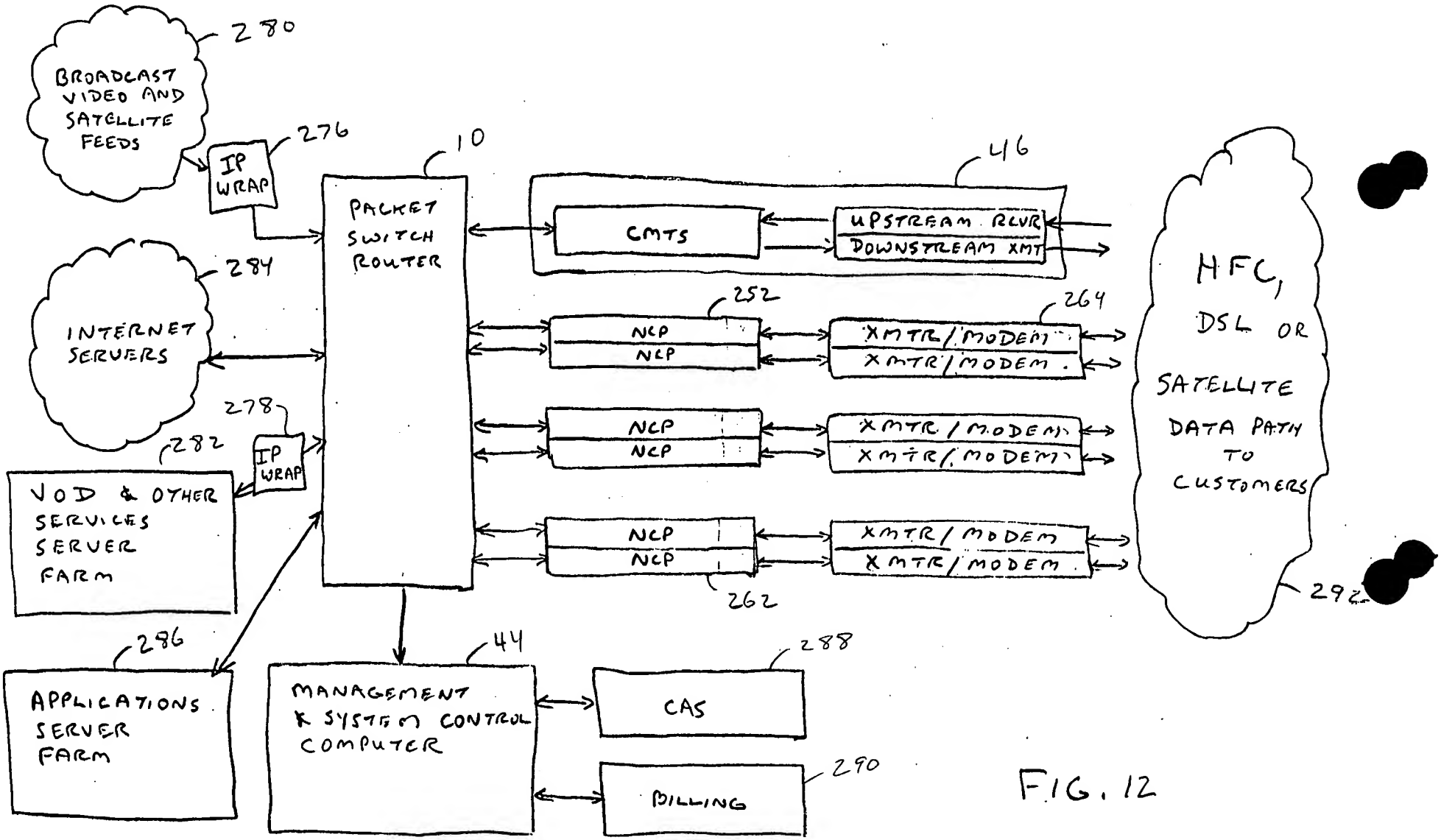


FIG. 12